



In our September Hot Topic '[Positioning](#)', we discussed the issues of designing a 3G (IMT2000) handset with an integrated GPS receiver - in particular, the challenge of decorrelating GPS and IMT2000 signals in the presence of IMT2000 transmit energy - a bringing together of RF and DSP design skills.

Previous Hot Topics have highlighted similar RF/DSP design performance trade offs, particularly in terms of receiver performance optimisation.

['Digital IF Design'](#) (June 99), defined the key performance parameters of the sampling A to D converter.

['3G Receiver Noise Budgets'](#) (September 99), analysed W-CDMA bit error rates, modulation bandwidth, data rate, spreading rate and spreading gain parameters and associated receiver noise floor performance.

['3G Demodulation Budgets'](#) (October 99), established the carrier to noise ratio (CNR) required at the input to the demodulator.

['W-CDMA Processing Gain'](#) (November 99) quantified the benefits of processing gain in the required CNR through the IF stages and the related relaxation of ADC resolution.

['3G DSP'](#) (December 99) looked at RF/IF processing before analogue to digital conversion and post processing after signal conversion.

Given that over 18 months have passed since we last visited this subject, we thought it was time to re-look at some of the RF and DSP trade offs involved, but this time to focus on Tx implementation.

DSPs have traditionally been used (and will continue to be used) for the standard baseband tasks of source coding, channel coding and PN code generation. (Fig 1)

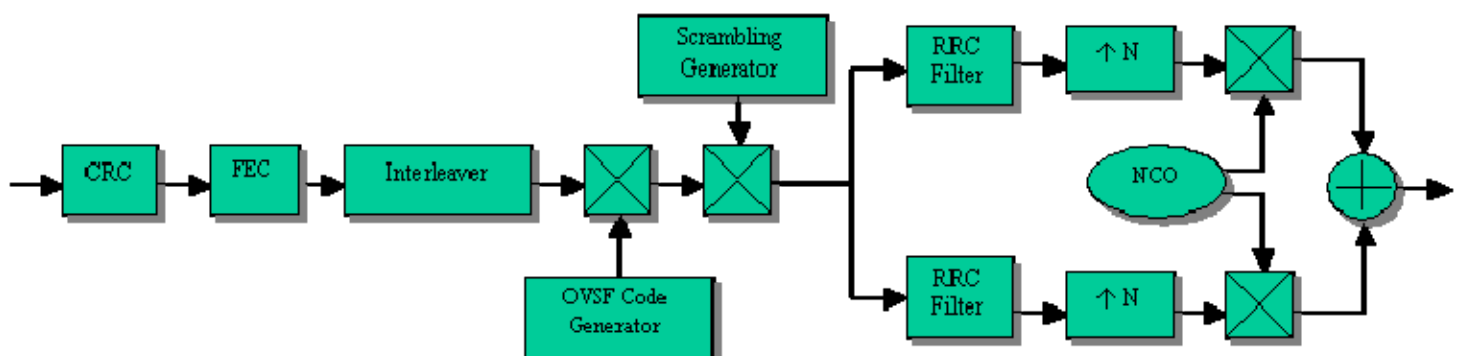


Fig 1: Baseband Processing Tasks

The 'new' tasks taken on by the DSP now however include digital filtering, frequency selection, IQ modulation and pre-distortion (to help optimise RF PA performance). The result is that it is now much more important for DSP and RF designers to work together on performance specification.

In terms of the digital filter, the prime characteristics have to include very linear phase and a good (low) shape factor.

The direct digital synthesiser provides frequency selection precision within a fraction of a herz and a fast settling time.

The IQ modulator has to provide good amplitude and phase balance (better than 70 db image suppression).

Because the sample rate of D/A converters is still not sufficiently high to allow direct translation to the final RF frequency in the digital domain, and because D/A convertors still tend to be power hungry, some analogue frequency translation and LO generation is needed to meet performance and power constraints. The selection of the digital IF to be used, and the relationship between digital LO generation/step size and analogue synthesiser parameters is an area where good discussion and planning between the DSP designers and analogue designers is an essential pre-requisite for producing a phone that meets specification.

Likewise with PA linearisation (Fig 2). The 3G specifications require between 30 and 35 dB third order intermodulation performance for handsets. Achieving this with an unlinearised amplifier is possible, but with only about 25% to 30% efficiency. Comparing this with 55% efficiency for state of the art GSM handset amplifiers highlights a significant shortfall which must be overcome by a combination of better device technology, better PA design, and external linearisation.

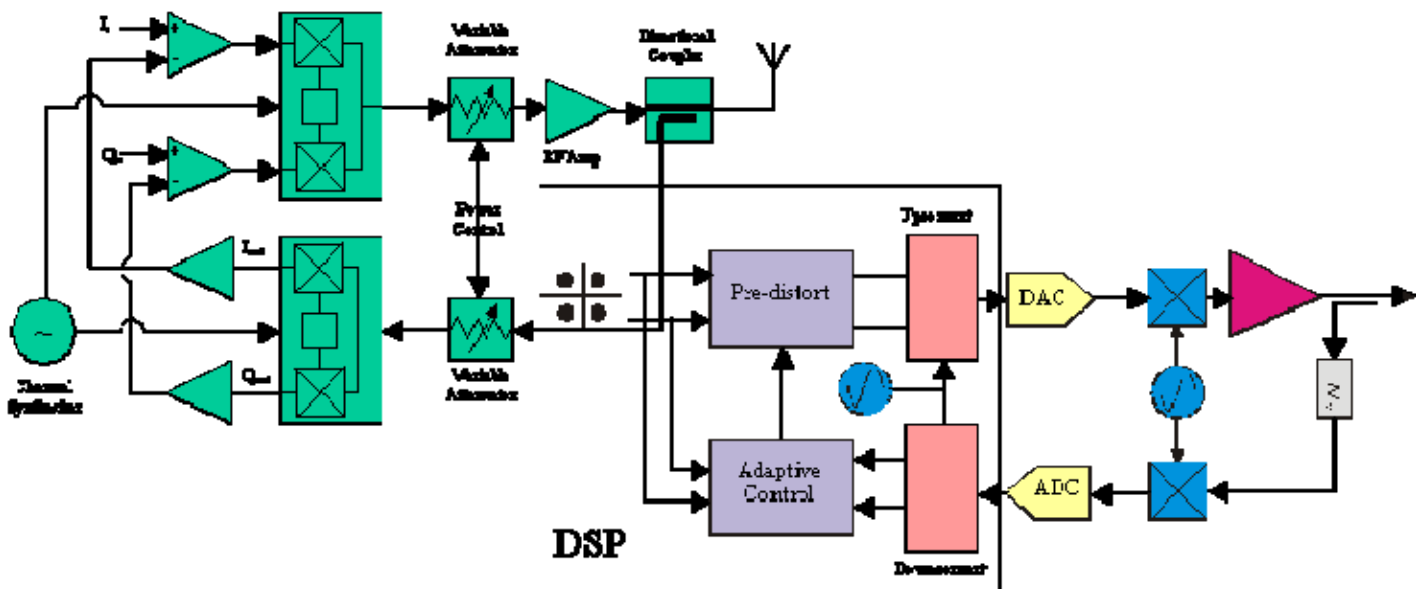


Fig 2: The Role of the DSP in PA Linearisation

Practical alternatives to RF synthesis include **Cartesian loop** - a linearisation technique that works well with narrow modulation bandwidths, but gives only limited processing gain (<10dB) at 3G

modulation bandwidths.

**Adaptive Pre-Distortion** at both RF, IF and baseband (digitally) can give very worthwhile intermod improvement (approx 5 to 10 dB uncompensated, and up to 20dB to 25dB with feedback control) over several MHz of bandwidth.

The generally acceptable compromise for a handset is to use a combination of pre-distortion and adaptive control which increases efficiency to between 40 and 45%, reasonably close to the GSM 55% efficiency benchmark.

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If you would like more information on this work then please contact

[geoff@rttonline.com](mailto:geoff@rttonline.com)

00 44 208 744 3163