RTT TECHNOLOGY TOPIC
January 2004

Media Processor Design

This month's Hot Topic focuses on power optimised media processor design - ie the design issues implicit in specifying and implementing power efficient microprocessors for multi-media hand held devices.

First some definitions - a media processor is a processor dedicated to simultaneously handling several multi-media data types and or data streams typically using an M-PEG4 and H.263 encoder/decoder. A media processor may also be described as an application processor. Usually an application processor is a media processor with a Java hardware accelerator. The processor will support media related applications like gaming, 3D processing, authentication and the housekeeping needed for J2ME personal profiles and MIDP (**m**obile **i**nformation **d**evice **p**rofiles).

Examples of media processors include products from Amphion, Emblaze (presently working with TTP on reference designs), Hantro (used in Motorola's i.MX21 platform, RealNetworks, PacketVideo (whose network division is now owned by Alcatel), MediaQ (now part of Nvidia), Neomagic, ST Microelectronics (Nomadik), TI (OMAP 732), Intel (Xscale/Bulverde processor), Samsung (S3C2440), Renesas (Hitachi SH-Mobile with Nazomi Java accelerator), Analog Devices Blackfin (including support for Windows Media Video 9) and Epson with their mobile graphics engine. Possible future vendors include Philips (Tri-Media), Infineon (Tri-Core), and AMD (presently active in PDA devices). and Equator (a major player in performance rather than power optimised media processing). Some of these devices are optimised for streaming video (RealNetworks for example), and some for real-time video (PacketVideo).

Most of these devices are ARM based with the exception of Renesas (the SH mobile widely used in FOMA phones) and possible future MIPS based processor designs. Essentially, there are two approaches to delivering performance and power efficiency. Vendors such as Intel and Samsung use fast clock speeds to get performance and then (using Intel as an example), implement voltage and frequency scaling to reduce power drain. Usually, the application processors clock at a multiple of the original GSM clock reference on the basis that the devices will be used in dual mode GSM/UMTS handsets. The Intel device frequency scales from 156 to 312 MHz and the Samsung device scales up to 533 MHz (13 times 13 MHz). Consider that most baseband processors tick along at 52 MHz (3 times 13 MHz) and you get an idea of the additional processor load being introduced to support multi-media functionality.

Other vendors such as Neomagic have highly optimised massively parallel architectures to improve throughput and reduce latency, jitter and power drain. In conventional device architecture, you get about one MIP per MHz. Handling high quality M-PEG4 with good light handling capabilities requires about 650 MIPS, handling H264 QVGA at 15 frames a second requires about 750 MIPS, handling continuous speech recognition requires about 1000 MIPS. The claim from Neomagic is that a massively parallel architecture (512 ‘words’ per clock cycle) can deliver 1200 ‘effective MIPS’ from a 200 MHz ARM 9 device.

Given the diversity of media processors presently being sold or sampled to handset manufacturers and the present diversity of vendor solutions, there is an apparent need to try and standardise the hardware and software interfaces used in these devices and to provide some form of common benchmarking for processor performance. The MIPI (**M**obile **I**ndustry **P**rocessor **I**nterface) alliance www.mipi.org established by TI, ARM, ST and Nokia is presently working on developing an industry standard for power management, memory interfaces, hardware/software partitioning and peripheral devices, though the OMAP heritage behind MIPI may hinder industry wide acceptance .The **E**mbedded **M**icroprocessor **B**enchmark **C**onsortium www.eembc.org is working on a J2ME benchmark suite with a set of standardised processor tasks (image decoding, chess, cryptography) so that processors can be compared in terms of delay, delay variability and multi-tasking performance.

Part of the benchmarking process has of course to address the issue of video quality, which in turn is complicated by the fact that different vendors use different error concealment techniques. One of the reasons GSM voice calls are reasonably consistent in mobile to mobile calls is due to the fact that error concealment is carefully specified across the range of codecs presently available (Full rate, enhanced full rate and adaptive multi rate). M-PEG4 however permits substantial vendor differentiation in the way that error concealment is realised which will lead to a lack of consistency in video mobile to mobile. A problem that network operators would sooner not have to deal with.

Irrespective of the success or otherwise of the standards making process, there are some fundamental decisions needed on processor architectures which depend on a number of assumptions being made on processor load, efficiency and multi tasking capability.

Figure 1 puts some of these decisions into a system context. Consider a power optimised multi-tasking multi-threaded media processor in a handheld device, specifically a 3G W-CDMA/UMTS handheld device.

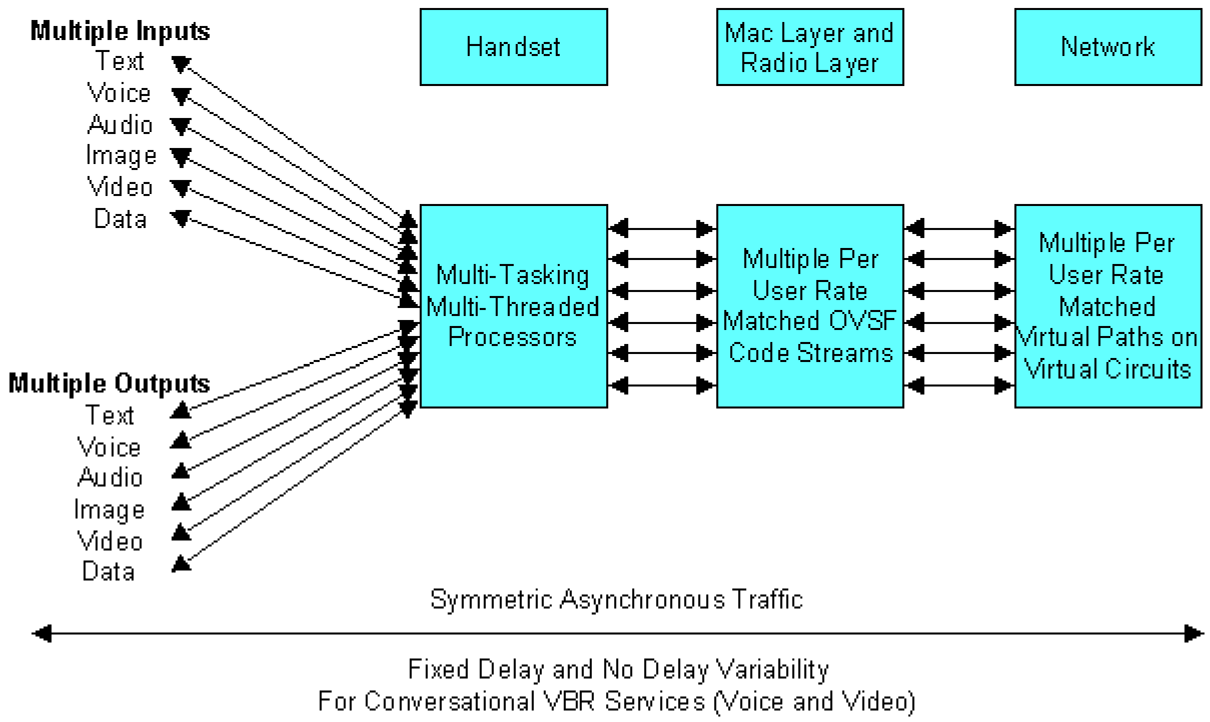

Figure 1: Power Optimised Media Processor Design

The core has to be capable of handling multiple inputs and outputs including text, voice, audio (including **high quality** audio), image, video and data. For conversational variable bit rate traffic (a small but significant percentage of the future traffic mix), the processor has to maintain the time interdependency between the input and output data streams. In effect, the processor must act as a real time operating system in the way that it handles multiple media streams into, across and out of the processor core.

The same level of determinism then needs to be applied to the MAC and physical radio layer, preserving the time interdependency of the multiple per user rate matched OVSF code streams and then on into the network with multiple per user rate matched virtual paths and circuits.

Note that together, the handset media processor, MAC layer and radio layer and network transport have to deliver tightly managed fixed delay and no delay variability, a requirement inconsistent with many existing processor cores.

Processor loading is also generally being considered in terms of asymmetric loading - ie a higher processor load on the downlink (from network to mobile).

This assumption is really not appropriate for conversational VBR services which are, and always will be symmetric in terms of their processor load - a balanced, though highly asynchronous, uplink and downlink.

Note also that a balanced uplink/downlink implies a higher RF power budget for the handset. Most RF power budgets assume that the handset will be receiving more data than it is transmitting which is just not the case. A higher RF power budget in the handset places additional emphasis on processor and RF PA power efficiency. Given this, one of the most useful benchmarks for a video handset will probably be its milliamp/hour per Megabyte performance under specified channel conditions. Given that the milliamp/hour per Megabyte metric effectively determines network loading and margin, this could turn out to be one of the most important measures of phone (and processor) performance.

The moral of the tale is not to take architectural decisions at processor level without a close look at system level issues!

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